THALIA
DESIGN AUTOMATION LTD

CUSTOMER CASE STUDY - RAPID GENERATION OF A FAMILY OF LDOs

GENERATE A FAMILY OF 100MA, 200MA, 500MA AND 1A LDOs FROM AN EXISTING 20MA DESIGN

Thalia deployed its innovative design automation technology and deep experience of analog design to migrate a 20mA low drop-out regulator (LDO) design to a new process node, and to create multiple design variants, allowing the customer to quickly and cost-effectively diversify its product range, and to use the most appropriate manufacturing technology available. Thalia's unique approach saved the customer more than 60% in design time.

Business issue and need

LDOs, along with voltage reference circuits, are among the basic building blocks in SoC design. A typical SoC like a Bluetooth or a WiFi IP may have four or more LDOs to address different load requirements.

In this case, Thalia's customer had an urgent requirement to generate a family of LDOs based on a proven design from an existing SOC for a new product.

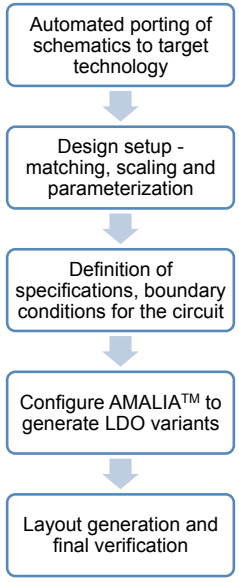
Typical timescales to design a LDO are of the order of a few weeks. The project timescales did not support the six man-weeks the customer expected the porting and variants generation to take; neither did they have resources free to undertake this effort.

An existing LDO was migrated from a TSMC 0.13µm process to an AMS 0.35µm process to generate a family of LDOs using Thalia's AMALIA™ design automation flow.

The baseline production qualified 20mA LDO was silicon proven from an existing SoC.

Thalia's solution

The first step was the porting of design schematics from the original TSMC 0.13µm process to the target process using Thalia's automated porting capability.



Once the mapping files were configured, the automated schematic porting effort generated the final schematics rapidly. The next step was identifying components within the design that needed to be configured before AMALIA could be deployed. This step was driven by one of Thalia's experienced analog designers, who understood the circuit characteristics and defined functional boundaries for the four LDO variants. Components like differential pairs, current mirrors and load devices were matched, scaled and parameterized in line with circuit requirements.

AMALIA incorporated the design information defined during the circuit customization process and leveraged an industry standard simulator (Spectre®) to identify potential solutions that met all the circuit specifications. The search space for this use case was about 10^{130} data points. A completely manual approach would have taken several man weeks.

By deploying AMALIA alongside an experienced analog design resource, Thalia was able to generate the LDO family in less than two man-weeks, four man weeks less than would have been possible using internal engineering resources, reducing both the project timescale and the overall cost to the customer.

Figure 1: the flow deployed in the development of the LDO variants.

Technium Springboard Centre | Cwmbran | NP44 3XF | UK

THALIA
DESIGN AUTOMATION LTD

LDO CASE STUDY

Summary and conclusion

Schematic porting of the LDO from the original technology to the target process node was performed using Thalia's schematic porting capability.

Thalia deployed the AMALIA analog design automation flow and an experienced analog designer to successfully create the variants of the 20mA LDO. The new variants met or exceeded all of the customer's design requirements. The no load current and dropout voltage were prioritised and were weighted to be as low as possible during the LDO variants generation process.

All of this was achieved while simultaneously saving the customer more than 60% in design time, accelerating the overall project and cutting engineering costs.

Specification	Unit	Spec Min	Spec Typ	Spec Max	20mA LDO	100mA LDO	200mA LDO	500mA LDO	1000mA LDO
VBAT Supply Voltage	V	2.7		3.6	2.7 – 3.6 V	2.7 – 3.6 V	2.7 – 3.6 V	2.7 – 3.6 V	2.7 – 3.6 V
Dropout Voltage	mV		50 mV	150 mV	65.3 mV	136.4mV	83.4mV	144.7mV	62.1mV
Current no Load	µA		5	25	3.65 µA	6.37uA	3.14uA	3.57uA	4.30uA
Sleep regulated Voltage	V	1.6			2.21 V	2.20V	2.21V	2.21V	2.20V
Regulated Voltage	V		2.2 V		2.21 V	2.20V	2.20V	2.20V	2.19V
Load Regulation	mV	-35		35	4.9 mV	1.32mV	28.74mV	2.79mV	-21.75mV
Line Regulation	mV	-15		15	0.21 mV	0.11mV	0.56mV	0.26mV	-6.23mV
PSRR @ DC	dB	-90 dB			-105.7dB	-99.8dB	-94.6dB	-94.7dB	-95.0dB
PSRR @ 200Hz	dB	-90 dB			-105.5dB	-99.8dB	-94.5dB	-94.7dB	-95.0dB
PSRR @ 1MHz	dB	-45 dB			-46.8 dB	-49.5dB	-46.3dB	-45.0dB	-46.5dB
# of Candidates					64	160	64	416	192

THE THALIA APPROACH

Thalia's approach to customers' analog and mixed signal design projects combines the experience and expertise of our design team, with the use of AMALIA - our proprietary and highly innovative design automation technology.

Our unique combination of expertise and analog design automation allows us to cost-effectively undertake development projects on behalf of our customers, with multiple benefits:

- Faster project turnaround
- More cost-effective than using customers' internal engineering resource
- Allows internal teams to focus on innovation and value-add

The AMALIA design enabling software:

- Assists in porting of schematics from one technology to another
- Supports our design team in validating and centering their design post migration
- Enables the generation of circuit variants: eg low power, different loads, or area-optimization
- Enables rapid qualification of the circuit topology in a new process node
- Facilitates analysis and understanding of the impact of trading off circuit characteristics

AMALIA tightly integrates into the Cadence® framework and leverages industry standard simulators such as Spectre, APS, Eldo and AFS.

Technium Springboard Centre | Cwmbran | NP44 3XF | UK