Generate a Bandgap derivative with a smaller area for a UK Design house

Amalia reduced the component area of this circuit by 57.5% while also meeting the requirements for current.

Specification	Requirement		Customer Design	Thalia Solution 1	
	Minimum	Typical	Maximum		
Supply Current	-	180 μΑ	-	180.29 μΑ	157.42 μΑ
Bandgap Circuit Current	-	75 μΑ	-	75.38 μΑ	52.615 μΑ
StandBy Current	-	100 nA	-	10.05 nA	5.02 nA
VGB Variation Trimmed	-	1.199 V	1.202 V	1.199 V	1.197 V
VGB Variation Trimmed Minimum	-	1.199 V	1.202 V	1.198 V	1.196 V
VGB Variation Trimmed Maximum	-	1.199 V	1.202 V	1.2 V	1.198 V
VGB Variation Mismatch	0.3 %	-	-0.3 %	+/- 0.3 %	+/- 0.3 %
Bandgap Current Variation Mismatch	10 %	-	-10 %	-16.82% to 11.01%	-9.8% to 12.03%
Vbg Variation over Trim Current at 5μs, 7μs, 10μs,					
15μs, 25μs, 35μs, 45μs	1.07 V	-	1.42 V	-1.19 V to 1.43 V	1.197 V - 1.203 V
Pmos Currents at 5μs, 7μs, 10μs, 15μs, 25μs, 35μs,					
45μs	8.35 μΑ	10 μΑ	12.4 μΑ	9.93 μΑ - 9.99 μΑ	9.98 μΑ - 10.05 μΑ
Nmos Currents at 5μs, 7μs, 10μs, 15μs, 25μs, 35μs,					
45μs	4.17 μΑ	4.99 μΑ	6.16 μΑ	4.98 μΑ - 5.01 μΑ	4.88 μΑ - 5.93 μΑ
Startup Time	2.13 μs	2.29 μs	2.96 μs	2.311 μs	2.179 μs
Pmos Currents Settling Time	3.8 μs	4.1 μs	5.5 μs	4.31 μs	2.855 μs
Nmos Currents Settling Time	3.8 μs	4.1 μs	5.5 μs	4.02 μs	2.992 μs
PSRR (< 1 KHz)	-	-	-50 db	-65.59 db	-56.9 db
PSRR (< 100 KHz)	-	-	-30 db	-35.9 db	-37.9 db
PSRR (> 100 KHz)	-	-	-20 db	-29.9 db	-27.4 db
PSRR (> 10 MHz)	-	-	-20 db	-32.55 db	-52.8 db
Startup Circuit Phase Margin	89°	92°	95°	91.4°	89.01°
Startup Circuit Gain Margin	37 db	38 db	39 db	37.99 db	35.5 db
Bandgap Loop Phase Margin	73°	75°	77°	77.02°	69.46°
Bandgap Gain Margin	22 db	25 db	31 db	28.19 db	20.3 db
Component Area	-	-	-	22927 μm²	9759 μm²
Solutions Evaluated*	-	-	-	-	800**

^{*}Average number of simulated solutions required to reach the first optimised solution

^{**}Simulation time for each solution is apprximetly 1 minute. The total time using four simulators in parallel is 3 hours and 30 minutes

