Two stage amplifier in cmos32lp

The focus here was to meet the requirements for GBW and Differential Phase Margin Freqency while also reducing current and component area.

Specification	Requirement	Customer Design	Thalia Solution
Differential Phase Margin Angle	>45°	52.99°	50.24°
Component Area	-	2500 μm^2	851.83 μm^2
Differential Phase Margin Frequency	>500 MHz	407.91 MHz	535.23MHz
Differential Open Loop Gain at 100 kHz	>50 db	64.61 db	63.93 db
GBW	>500 MHz	437.61 MHz	574.69 Mhz
DC Current	<1.5 mA	1.33 mA	1.15 mA
Input noise at 100 kHz	<60 nV/√Hz	53.51 nV/√Hz	52.14 nV/√Hz
Input noise at 10 MHz	<60 nV/√Hz	60.39 nV/√Hz	47.33 nV/√Hz
Common Mode Phase Margin	>45°	53.14°	54.36°
Common Mode Phase Margin Frequency	>35 MHz	42.9 MHz	49.45 MHz
Solutions Evaluated*	-	-	320**
*Average number of simulated solutions required to reach the first optimised solution			
**Simulation time for each solution is apprximetly 2 minutes. The total time using four			

Thalia